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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

DATE:	6/5/2006
IN RE APPLICATION OF:	ALAN R. BALL ET AL.
APPLN. NO.:	10/813501
FILED:	3/31/2004
FOR:	METHOD OF FORMING A SELF-GATED TRANSISTOR AND STRUCTURE THEREFOR
GROUP:	2816
EXAMINER:	QUAN TRA
	571-272-1755

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BY Robert Hightower ON: 6/5/06
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REPLY BRIEF UNDER 37 CFR 1.193(b)(1)

This Reply Brief is submitted in response to the arguments submitted in the Examiner's Answer mailed on April 17, 2006. Applicant respectfully request that arguments included hereinafter be included in any reconsideration of the application and when considering the arguments on Appeal and in the Examiner's Answer.

I. RESPONSE TO EXAMINER'S ARGUMENTS

Applicant disagrees with the positions stated in section 10 of the Examiner's Answer relating to claims 1-7, claims 8-11, and claims 12-20. To withstand a rejection under 35 USC 102, a reference must teach each and every aspect of the claimed invention either explicitly or impliedly. Any feature not directly taught must be inherently present. *MPEP section 706.02.* In relying on the theory of inherency, it is necessary that the inherent characteristic must necessarily flow from the teaching of the applied prior art. *Ex parte Levy, 17 USPQ.2d 1461, 1464 (P.O.Bd.Ap 1990).* Inherency, however, may not be established by probabilities or possibilities. *Ex parte Skinner, 2 USPQ.2d 1788, 1789 (P.O.Bd.Ap 1986).* The mere fact that certain thing may result from a given set of circumstances is not sufficient. *Id.* It is not proper use of a patent as a reference to modity its structure to one which the prior art reference does not suggest. *In re Randol and Redford, 165 USPQ 586, 588 (CCPA 1970).*

In the first paragraph of section 10, the Examiner's Answer attempts to modify the teaching of the cited reference (U.S. patent no. 5,936,440 issued to Asada et al ("Asada")). As applicant stated in the Appeal Brief, Asada teaches that the reference voltage described in column 6, lines 21-22, is "negative and nearly ground potential". Asada never discloses what the term "nearly ground" potential means. The Examiner's characterization that "nearly ground" could mean less than 1/10 of a milli-volt is not supported by Asada. This is merely speculation that is not supported by the relied on reference, thus, is an improper modification of the reference. Applicant's respectfully submit that the reference voltage being 1/10 of a milli-volt is also not an inherent feature that necessarily flows from the teaching of the reference. Thus, the technical explanation based on the reference voltage being such a value is

not supported by Asada and is not inherent to the teaching of Asada.

Further, the position in the Examiner's Answer is contrary to the teachings of Asada. Asada teaches in column 6, lines 23-34, that a negative current (backflow current) begins flowing through body diode 100 of transistor 10 to coil 32. This current forms the voltage Vs that is used to enable transistor 10 to reduce the resistance and more efficiently enable the negative current to flow from ground through transistor 10. Thus, this voltage is used to enable transistor 10. Asada teaches in column 3, lines 57-65, that a high level of control signal Vc is received by circuit 7 and is used to disable transistor 10. Note in FIG.s 4 and 5 that the output of comparator 840 is received by circuit 7 and that circuit 7 also receives signal Vc. Thus, as disclosed by Asada, circuit 7 is the circuit that controls disabling transistor 10 and that such disabling is responsive to a high level from signal Vc not from the output of comparator 840.

In conflict with the teaching of Asada, the Examiner's Answer argues that as the negative current discharges the field coil 32, that an input offset voltage and a delay will allow the current to become positive. Applicant respectfully submits that this is also a modification of the reference that is not supported by the teaching of the reference. Additionally, such a modification is not an inherent result that necessarily flows from the teaching of the reference, there are any number of results based on the comparator having an input offset voltage and the gate having a delay. In fact, Asada teaches the opposite by teaching in column 3, lines 56-63, that transistor 10 is turned off by a high level of signal Vc. Asada never teaches or implies that transitory 10 is disabled by comparator 840. The Examiner's Answer states that Asada's comparator 840 has an input offset voltage that causes it to not change state immediately after the voltage potential at its negative input terminal

reaches the negative value of reference Vr and cites to Millan et al for support. Applicant respectfully submits that even if the Asada comparator 840 had an input offset voltage, that a person of ordinary skill in the art is aware of the input offset voltage of comparators and would choose a comparator with an input offset voltage that provides the performance that is cited in the Asada reference. Discrete comparators, like the one cited in Millian et al, are available with numerous different input offset voltages and an appropriate one could be selected. Millian et al merely explain one particular offset voltage of one particular comparator. Further, the Asada comparator 840 is formed on an integrated circuit. Integrated circuit engineers routinely adjust the input offset voltage of a comparator to obtain the desired comparator operation. Additionally, a person of ordinary skill in the art would adjust the value of the Vr voltage to compensate for such an input offset voltage in order to obtain the results disclosed by the Asada reference. Thus, applicants respectfully submit that the position put forth in the Examiner's Answer is not supported by the Asada reference and is also not an inherent characteristic that necessarily flows from the teaching of Asada. Accordingly, Asada does not disclose that comparator 840 detects a positive voltage and disables transistor 10.

Additionally, the Examiner states that comparator 840 and gate 501 have delays that prevent transistor 10 being turned off until the current through transistor 10 turns positive. Applicants again respectfully submit that this position is not supported by Asada nor by any legal theory under 35 USC 102. A person of ordinary skill in the art could again change the value of the reference voltage Vr to make sure that comparator 840 changed state as describe in the Asada reference. Thus the position put forth in the Examiner's Answer is not supported by Asada nor by the doctrine of inherency.

In the second paragraph of section 10 and relating to claim 19, the Examiner's Answer states that the battery is a vehicle battery that is a constantly charged voltage source and is regulated by the vehicle engine. Applicant respectfully disagrees. Asada teaches in column 2, lines 49-50, that element 3 is the vehicle alternator and that element 4 is a control apparatus that controls alternator 3. Asada further states in column 1, lines 65-67, that the first control circuit (4) regulates the battery voltage by turning on or off the high-side switching element. Thus, control apparatus 4 is the voltage regulator that regulates the charging of the vehicle battery. Asada does not disclose any other voltage regulator than apparatus 4. Since transistor 10 and comparator 840 are a part of apparatus 4, apparatus 4 can not be a voltage regulator, separate from the regulator that includes comparator 840 and transistor 10, that provides the operating voltage to comparator 840. Accordingly, this position of the Examiner's Answer directly conflicts with the teachings of Asada.

Respectfully submitted,
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